**DAILY ASSESSMENT FORMAT**

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| **Date:** | **03- June- 2020** | **Name:** | **Varun G Shetty** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC093** |
| **Topic:** | •  **EDA Playground Online complier** •  **EDA Playground Tutorial Demo Video** •  **How to Download And Install Xilinx Vivado Design Suite** •  **Vivado Design Suite for implementation of HDL code** | **Semester & Section:** | **6th sem & B sec** |
| **Github Repository:** | **Varunshetty4** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session**  page1image32332704 |
| **EDA Playground Online complier:**  page2image32169280  **EDA Playground Tutorial Demo Video:**  page2image32169904  **How to Download And Install Xilinx Vivado Design Suite:**  page3image32250576  **Vivado Design Suite for implementation of HDL code:**  page3image32250992  **TASK:**  **Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.**  page4image32284176  **OUTPUT:**  page4image32284384 |